Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (currently amended) A transponder comprising:

a memory for storing data therein;

a clock generator for outputting a read signal for supplying current to the memory;

an address module for addressing ~~an~~ a selected address from a plurality of addresses in the memory, said clock generator outputting an increase address ~~clock~~ signal and said address module selecting an address to be read in response to ~~a~~ said increase address ~~clock~~ signal from said clock generator; and

a data module for receiving the data stored in said memory at ~~an~~ said selected address indicated by said address module and for latching said data in response to a latch data signal from said clock generator, said clock generator stopping supplying said read signal to turn off said current to said memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module, said current thus being cycled on and off with each latching of the contents of each successive selected memory address in ~~once said data has been output to~~ said data module.

2. (cancelled)

3. (original) The transponder of claim 1, wherein said clock generator outputs a program signal for supplying current to the memory to program the memory, and said address clock signal is an address latch signal, the address module selecting a specific address of the memory in response to the address latch signal, said data module inputting data to the memory at

the address indicated by the address module, said clock generator stopping supplying current to the memory once the data in the data module has been stored in the memory.

4. (original) The transponder of claim 1, further comprising a program control and said memory having a status byte region and a data region, said program control reading data from said status byte region and in response thereto, outputting a program enable signal to said clock generator to enable said clock generator to output said address signal to said address module.

5. (original) The transponder of claim 4, wherein said status byte region stores at least a first seal bit and a second seal bit, said program control reading said first seal bit and said second seal bit and outputting the program enable signal if at least one of said first seal bit and second seal bit is clear.

6. (original) The transponder of claim 4, wherein said status byte includes an HLOCK bit, said HLOCK bit being capable of being set or clear, said program control reading said HLOCK bit and receiving an address from said address module, and outputting said program enable if said HLOCK bit is clear or said HLOCK bit is set and said address output by said address module corresponds to the address of the status byte within said memory.

7. (Currently Amended) A transponder comprising:

a memory for storing data therein, said memory having addresses;

a clock generator outputting a program signal for supplying current to the memory to program the memory;

an address module for addressing ~~an~~ a selected address from a plurality of addresses in the memory, said clock generator outputting an address latched signal, said address module selecting ~~an~~ selected address to be read in response to the address latch signal; and

a data module for inputting data to the memory at the address indicated by the address module, said clock generator stopping supplying current to the memory each time the contents of a selected memory address from the plurality of addresses ~~once the data in the data module~~ has been stored in the memory, said current thus being cycled on and off with each storing of the contents of each successive selected memory address of the plurality of memory addresses in the memory.

8. (original) The transponder of claim 7, further comprising a program control and said memory having a status byte region and a data region, said program control reading data from said status byte region and in response thereto, outputting a program enable signal to said clock generator to enable said clock generator to output said address signal to said address module.

9. (original) The transponder of claim 8, wherein said status byte region stores at least a first seal bit and a second seal bit, said program control reading said first seal bit and said second seal bit and outputting the program enable signal if at least one of said first seal bit and second seal bit is clear.

10. (original) The transponder of claim 8, wherein said status byte includes an HLOCK bit, said HLOCK bit being capable of being set or clear, said program control reading said HLOCK bit and receiving an address from said address module, and outputting said program enable if said HLOCK bit is clear or said HLOCK bit is set and said address output by said address module corresponds to the address of the status byte within said memory.

11. (original) The interrogator of claim 1, wherein the clock generator outputs an address latch signal to said address module in response to a program signal from an interrogator, said address latch signal causing said address module to select an address to be programmed in accordance with said program signal, said program signal being pulse space modulated.

12. (original) The transponder of claim 6, wherein said status byte further includes a mode bit, said program control reading said mode bit and providing an output to said address module preventing said address module from accessing addresses in said memory not corresponding to the mode indicated by said mode bit.

13. (Currently Amended) A transponder comprising:

a memory, said memory including a data region and a status byte region;

a clock generator for receiving a program signal and outputting a data latch signal in response thereto;

an address module for receiving said address latch signal and addressing a predetermined address <u>from a plurality of addresses</u> in the memory to be programmed; and

a program control for reading said status byte and outputting a program enable signal in response thereto, said clock generator receiving said program enable signal and outputting said address latch in response to said program enable signal

a data module for receiving the data stored in said memory at an address indicated by said address module, said clock generator stopping supplying said read signal to turn off said current to said memory each time the data from a predetermined address ~~once said data~~ has been output to said data module, said current thus being cycled on and off with each outputting of the data of each successive address of the plurality of addresses.

14. (original) The transponder of claim 13, wherein said status byte region stores at least a first seal bit and a second seal bit, said program control reading said first seal bit and said second seal bit and outputting the program enable signal if at least one of said first seal bit and second seal bit is not set.

15. (original) The transponder of claim 13, wherein said status byte includes an HLOCK bit, said HLOCK bit being capable of being set or clear, said program control reading said HLOCK bit and receiving an address from said address module, and outputting said program enable if said HLOCK bit is clear or said HLOCK bit is set and said address output by said address module corresponds to the address of the status byte within said memory.

16. (previously presented) The transponder of claim 1, the transponder further comprising:

a comparator for receiving said interrogator signal and a reference voltage and outputting a first logic level if the voltage of the interrogator signal is greater than the reference voltage, and outputting a second logic level if the voltage of the interrogator signal is less than the reference voltage; and

a transmitter for receiving said first and second logic levels and outputting a first voltage indicator signal in response to said first logic level and outputting a second voltage indicator signal in response to said second voltage level, the first signal being the inverse of the second signal to indicate to an interrogator a received relative voltage level.

Claims 17-43 (canceled)

44. (original) The transponder of claim 1, wherein said transponder is formed as an integrated circuit and further comprising a clamp, the clamp including at least one MOSFET.

45. (original) The transponder of claim 44, wherein said clamp is formed by a CMOS process.

46. (previously presented) The transponder of claim 1, said transponder further comprising an integrated circuit, said integrated circuit including a clamp, the clamp including at least one MOSFET.

47. (Original) The transponder of claim 46, wherein said clamp is formed in a CMOS process.